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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,384	07/09/2003	Farshid Nowshadi	56162.000405	8500

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,384	NOWSHADI, FARSHID	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) *1,11,25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003 and 08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03,03/02/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 119(e).

2. Claims 1-25 are pending.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 8 December 2003 and 2 March 2004 were filed after the mailing date of the application on 9 July 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

4. Claims 1, 11, and 25 are objected to because of the following informalities: the word "map" is missing between "address is" in the last paragraph of each of the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3, 13, and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

7. As for claims 3 and 13, the specification does not teach that the method or system is capable of allowing each access of each of the plurality of different memory banks to overlap each other. For instance, the examiner does not see how two or more sequential accesses to a memory bank are capable of overlapping each other as claimed.

8. As for claim 24, the specification does not teach how the system is capable of comprising a central office as claimed.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1, 6, 11, 16, and 25 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. As for claims 1, 11, and 25, the phrase "distributed through" does not clarify to the examiner whether each of the plurality of different memory banks contains each of the memory address of the logical memory address, or each memory address of the logical memory address is distributed to one of the plurality of different memory banks.

12. As for claims 6 and 16, the term "improved" is a relative term which renders the claim indefinite. The term "improved" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1-8, 10-18, 20, 21, 23, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Leung et al. [US 6,895,488 B2].

15. As for claims 1, 11, and 25, Leung et al. discloses a method, a system (Fig 2, 100), and a mapping module, and a computer readable medium (Col 4, Lines 62-65) comprising a set of instructions (Col 2, Lines 15-17; Col 3, Lines 19-32) being adapted to manipulate a processor (Col 2, Lines 13-15) for improving access latency of multiple bank devices, wherein:

a plurality of different memory banks (Fig 2, 112a-112n) of a shared resource are identified (Col 2, Lines 24-28; Fig 2, 106) by an identifying memory banks module (Fig 2, 104);

a logical memory address map (Fig 2, ADDR_0-ADDR_N) of a processor accessing the shared resources is identified by an identifying address map module (Fig 2, 104); and

the logical memory address map is mapped (Col 3, Lines 29-32; Fig 2, 108, 104) to a shared resource address map (Fig 2, ROT_ADDR_0-ROT_ADDR_N) by a mapping module (Fig 2, 104) so that each memory address of the logical memory address is distributed through the plurality of different memory banks (Col 3, Lines 29-32; Col 3, Table 1; Col 4, Lines 47-48).

16. As for claims 2 and 12, Leung et al. further discloses that each memory address of the logical memory address map accesses each of the plurality of memory banks (Col 2, Lines 24-52; Col 3, Table 1).

17. As for claims 3 and 13, Leung et al. further discloses that each access of each of the plurality of different memory banks overlaps each other (Col 3, Table 1; Col 1, Lines 51; Col 5, Lines 4-8).

18. As for claims 4, 5, 14, and 15, Leung et al. further discloses that bursting cycles are not interfered, and the bursting cycles include efficient transfers of small sequential streams of data to a same memory bank (DMA, Col 1, Lines 50-54; Col 3, Table 1).

19. As for claims 6 and 16, Leung et al. further discloses that interleave accesses are improved (Col 1, Lines 47-54).

20. As for claims 7 and 17, Leung et al. further discloses that the plurality of memory banks comprise at least four different memory banks (Fig 2, 112a-112n; Col 3, Line 33; Col 3, Table 1).

21. As for claims 8 and 18, Leung et al. further discloses that the shared resource comprises one or more of DRAM, SDRAM and DDR (Col 1, Lines 53-54).

22. As for claims 10 and 20, Leung et al. further discloses that each of the four modules of the DSP accesses each of the four memory banks in rotation (Col 3, Table 1), which could only mean that the processor's local code must be spread across the plurality of memory banks.

23. As for claims 21 and 23, Leung et al. further discloses that the steps are performed in the system described above, which comprises a customer premise equipment (Col 2, Lines 10-21).

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al., further in view of Ware et al. [US 5,390,308]

26. Leung et al. already substantially discloses the method and system as described above, but does teach that the step of mapping or the mapping module further exchanges higher order address lines with mid-order address lines. However, Ware et

al. discloses a method and apparatus in which row bits of memory address are swapped with device identification bits to distribute neighboring memory accesses among banks of memory (Col 4, Lines 24-27), in order to decrease the latency incurred by frequent accesses to different rows in the same memory array/bank (Col 2, Lines 20-25). Also, the swapping of device identification bits with row bits is an exchange of higher order address lines with mid-order address lines (Fig 3a; Col 4, Lines 48-51). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention that Leung et al.'s system can lower its access latency by allowing the exchange of higher order address lines with mid-order address lines.

27. Claims 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung et al.

28. Leung et al. already substantially discloses the method and system as described above, but does not teach that the steps are performed at or the system comprises a central office. However, Leung et al. discloses that the invention can be implemented to perform intensive data processing (Col 2, Lines 15-20), which is one of the functions of a central data server that is physically located in an office. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention that the steps in Leung et al's method can be performed at a central office, and its system can comprise a central office.

Conclusion

29. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

Patent No:	
US 6,108,745	Fast and Compact Address Bit Routing Scheme that Supports Various DRAM Bank Sizes and Multiple Interleaving Schemes
US 2003/0046501 A1	Method for Interleaving Memory
US 6,745,277 B1	Intelligent Interleaving Scheme for Multibank Memory
US 6,587,913 B2	Interleaved Memory Device for Burst Type Access in Synchronous Read Mode with the Two Semi-Arrays Independently Readable in Random Access Asynchronous Mode
US 6,789,155 B2	System and Method for Controlling Multi-Bank Embedded DRAM

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

31 August 2005

GARY PORTKA
PRIMARY EXAMINER